AN2758
Application note

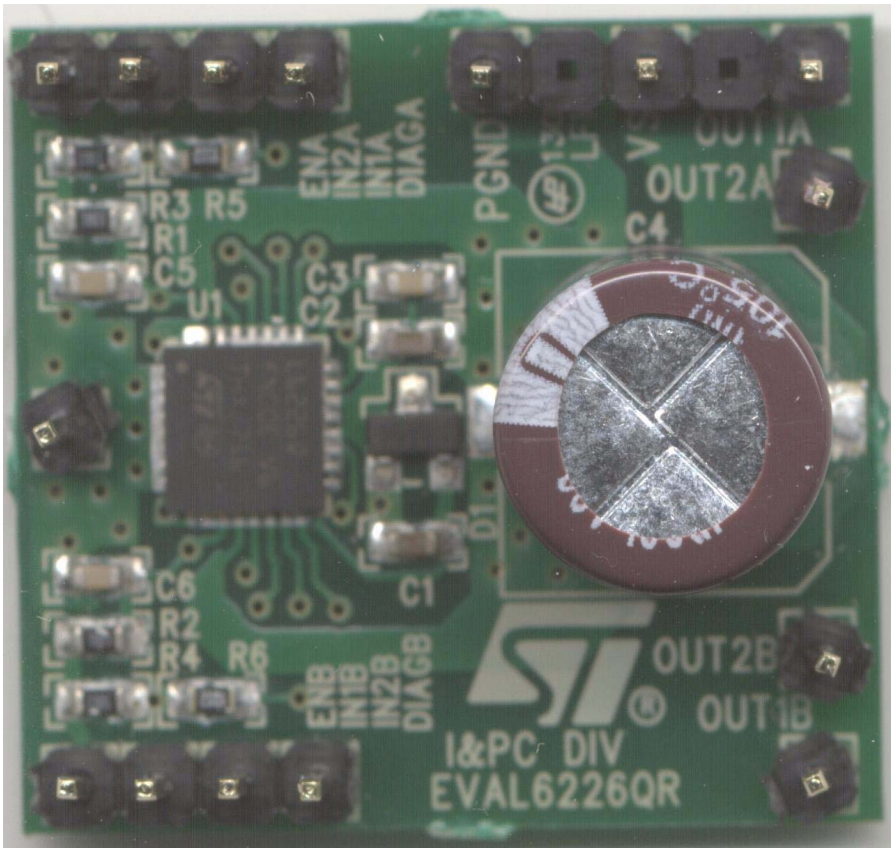
EVAL6226QR demonstration board using a dual full-bridge L6226Q for motor control applications

Introduction

This application note describes the demonstration board of the DMOS dual full-bridge L6226Q designed for motor control applications. The board implements a typical application that can be used as a reference design to drive two-phase bipolar stepper motors with currents up to 1A DC, multiple DC motors and a wide range of inductive loads.

Thanks to the small footprint of the L6226Q (QFN 5 x 5 mm, 32-lead) the PCB is very compact (27 x 24.5 mm).

Figure 1. EVAL6226QR demonstration board



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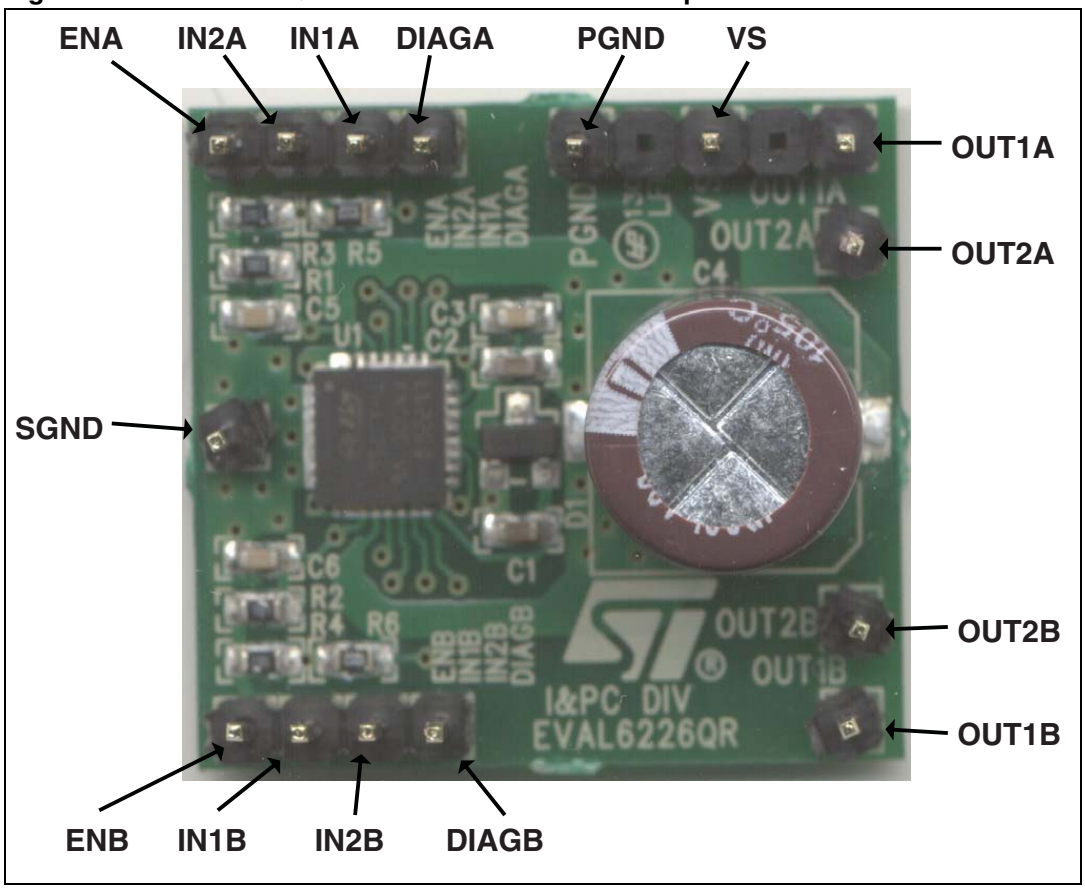
1 Demonstration board description

Table 1. EVAL6226R pin connections

Name	Type	Function
VS	Power supply	Bridge A and bridge B power supply
PGND	Ground	Power ground terminal
IN1A	Logic input	Bridge A logic input 1
IN2A	Logic Input	Bridge A logic input 2
ENA	Logic input	Bridge A enable (active high). When low, the power DMOSs of bridge A are switched OFF.
IN1B	Logic input	Bridge B logic input 1
IN2B	Logic input	Bridge B logic input 2
ENB	Logic input	Bridge B enable (active high). When low, the power DMOSs of bridge B are switched OFF.
DIAGA	Open drain output	Bridge A overcurrent detection and thermal protection pin. An internal open drain transistor pulls to GND when overcurrent on bridge A is detected or in case of thermal protection.
DIAGB	Open drain output	Bridge B overcurrent detection and thermal protection pin. An internal open drain transistor pulls to GND when overcurrent on bridge B is detected or in case of thermal protection.
SGND	Ground	Signal ground terminal
OUT1A	Power output	Bridge A output 1
OUT2A	Power output	Bridge A output 2
OUT1B	Power output	Bridge B output 1
OUT2B	Power output	Bridge B output 2

Figure 2. EVAL6226QR demonstration board description



The INx input pins drive the corresponding half-bridge. When low logic level is applied the low side MOS is switched on, whereas a high logic level turns on the high side MOS.

Pins ENA and ENB are used to implement overcurrent and thermal protection when connected respectively to the outputs DIAGA and DIAGB.

The output current detection thresholds are selected by the resistor connected between the IC dedicated pins and ground.

Table 2 summarizes the electrical specification of the application and *Figure 3* shows the electrical schematic.

Table 2. EVAL6226QR electrical specification (recommended value)

Parameter	Value
Supply voltage range (VS)	8 to 52 Vdc
RMS output current rating (OUTx)	up to 1.4 A
Switching frequency	up to 100 kHz
Input and enable voltage range	0 to + 5 V
OCD pins voltage range	-0.3 to 10 V
Operating temperature range	-25 to +125°C
L6226Q thermal resistance junction to ambient	22°C/W

Figure 3. EVAL6226QR demonstration board schematic

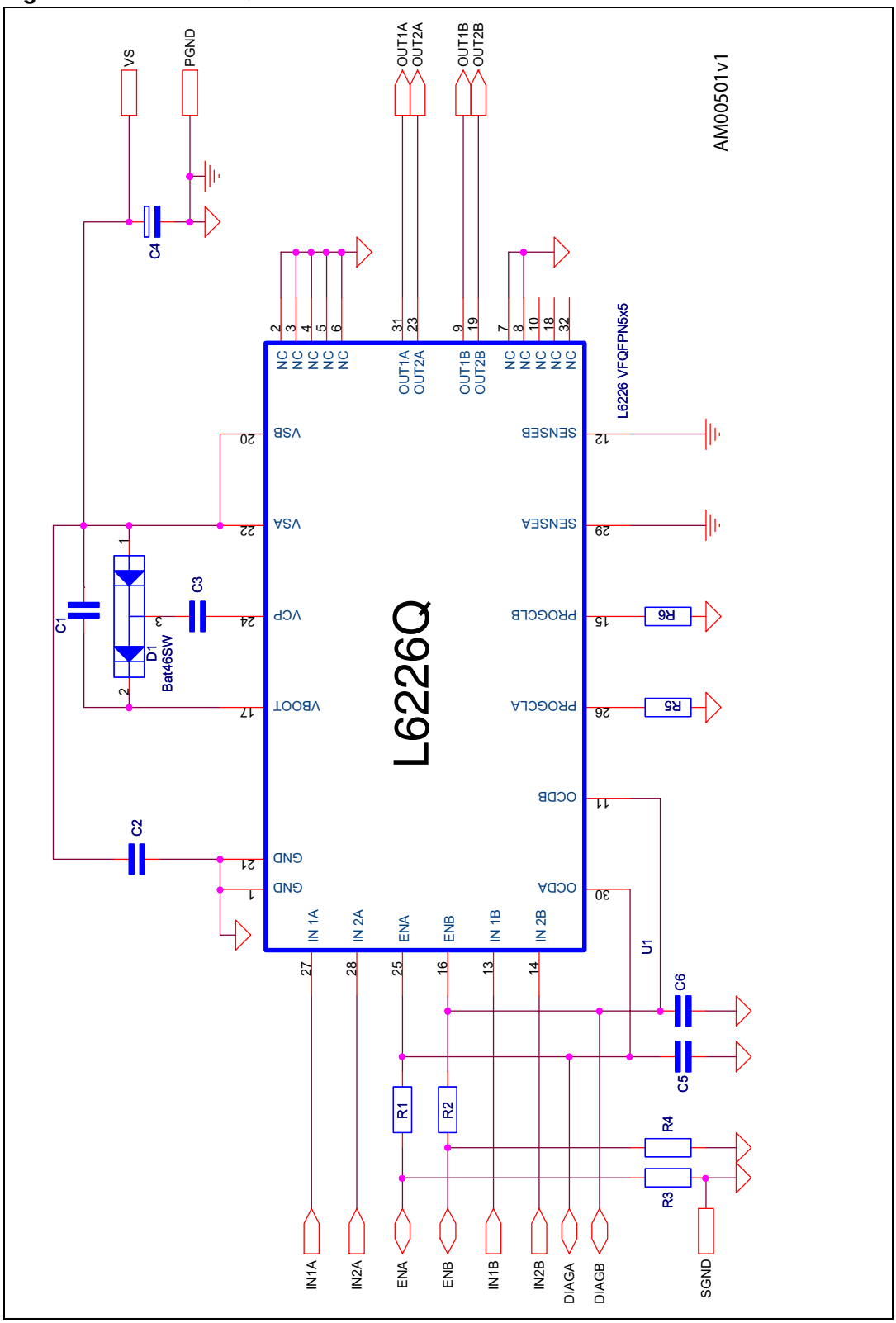


Table 3. EVAL6226QR part list

Part reference	Part value	Part description
C1	220 nF/25 V	Capacitor
C2	220 nF/63 V	Capacitor
C3	10 nF/25 V	Capacitor
C4	100 µF/63 V	Capacitor
C5, C6	5.6 nF	Capacitor
D1	BAT46SW	Diodes
R1, R2, R3, R4	100 kΩ 5% 0.25 W	Resistor
R5, R6	10 kΩ 1% 0.25 W	Resistor
R9, R10	0.4 kΩ 1 W	Resistor
U1	L6226Q	Dual full-bridge in VFQFPN5x5

D1, C1 and C3 constitute a charge pump circuit, which generates the supply voltage for the high-side integrated MOSFETs. Due to voltage and current switching at relatively high frequency, these components are connected through short paths in order to minimize induced noise on other circuitries.

R1, R2 and C5, C6 are used by the overcurrent protection integrated circuitry (disable time $t_{DISABLE}$ is about 200 µs and delay time t_{DELAY} about 1 µs using the values in *Table 3*).

R5 and R6 are used to set the output current detection threshold at about 1.1 A typical value. *Figure 4*, *Figure 5* and *Figure 6* show the placement of the components and the layout of the two layers of the EVAL6226QR reference design board. A GND area has been used to improve the IC power dissipation.

Figure 4. Component placement

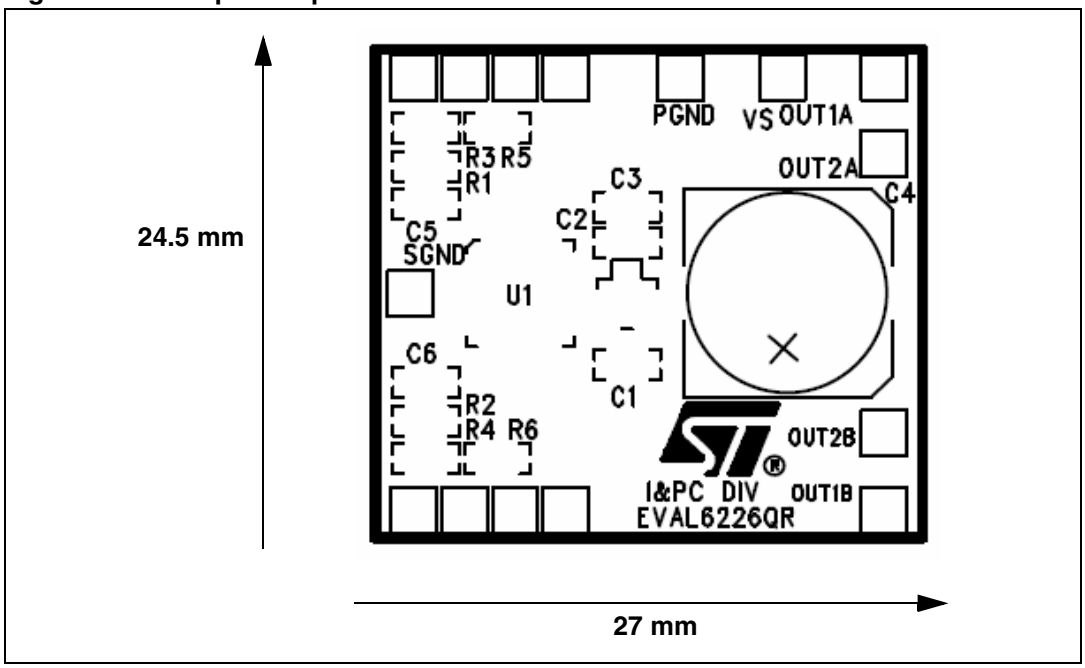


Figure 5. Top layer layout

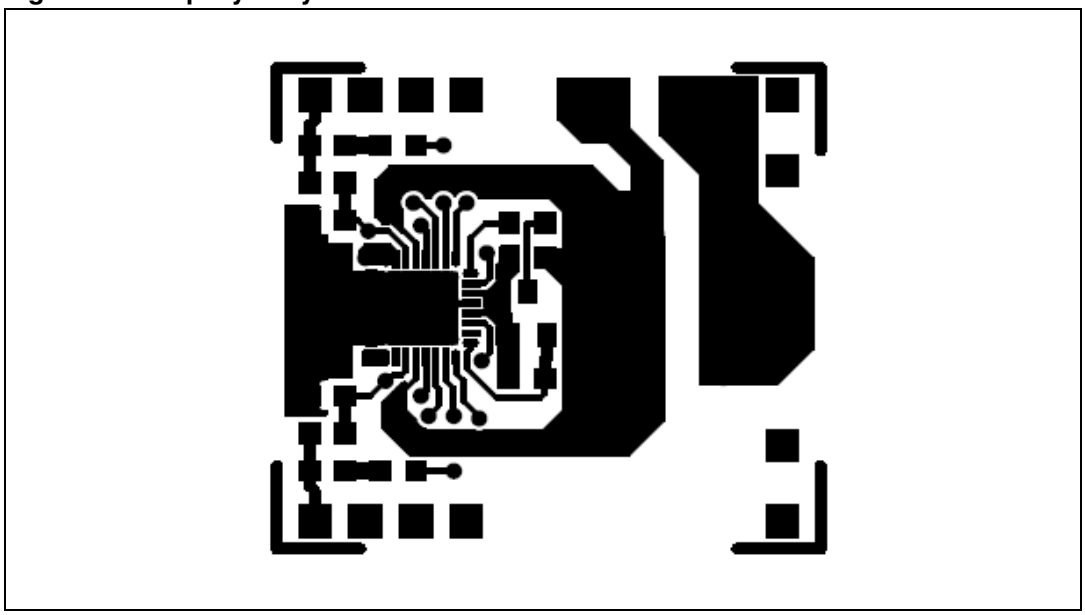
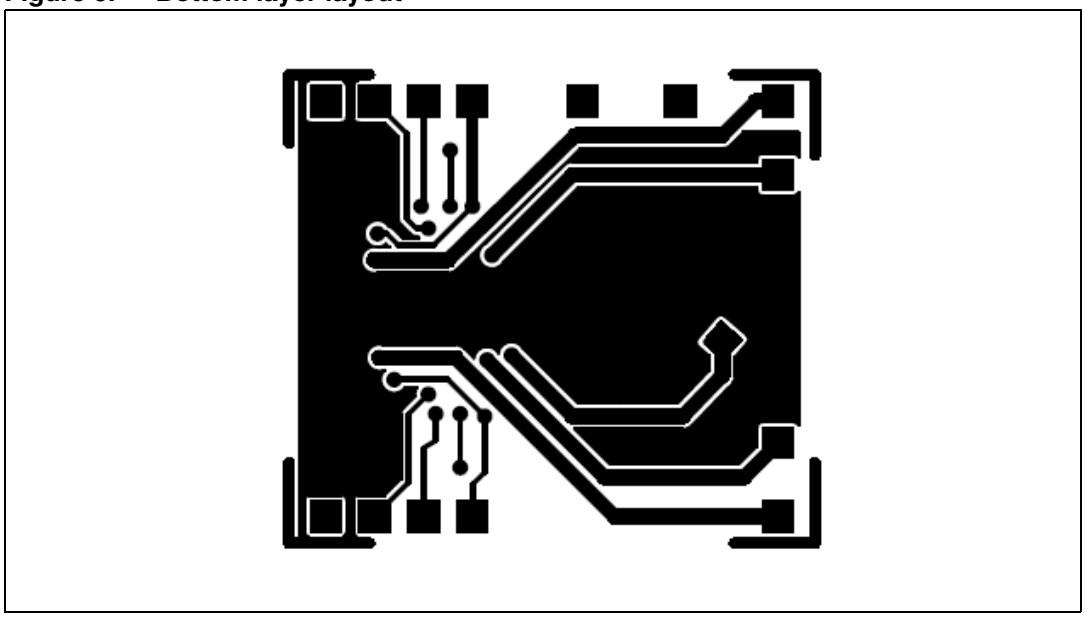


Figure 6. Bottom layer layout



2 Revision history

Table 4. Document revision history

Date	Revision	Changes
06-Oct-2008	1	Initial release